REMARKS

This Amendment is submitted in response to the Office Action dated October 31, 2003, having a shortened statutory period set to expire January 31, 2004.

In the present Amendment, Applicant has proposed amendments to rewrite Claims 17 and 18 in independent form and to cancel all other claims. Because the proposed amendments do not raise any new issues and necessarily reduce the outstanding issues by placing the claims in allowable form or in better form for appeal, Applicant believes that the proposed amendments are proper and respectfully requests entry of the proposed amendments.

In paragraph 5 of the present Office Action, Claims 3-4, 8, 10-11, 15 and 17-18 are rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. US 5,377,336 to *Eickemeyer et al.* (*Eickemeyer*). In addition, Claims 5 and 12 are rejected under 35 U.S.C. § 103(a) as unpatentable over *Eickemeyer*, Claims 6-7 and 13-14 are rejected under 35 U.S.C. § 103 as unpatentable over *Eickemeyer* in view of U.S. Patent No. 5,396,604 to *DeLano et al.*, and Claims 9 and 16 are rejected under 35 U.S.C. § 103 as obvious over *Eickemeyer* in view of U.S. Patent No. 5,931,957 to *Konigsburg*. Those rejections are respectfully traversed, and favorable reconsideration of the claims is respectfully requested.

Applicant submits that the present claims are not rendered unpatentable by *Eickemeyer* under 35 U.S.C. § 102 or § 103 because the cited references does not teach or suggest each claim feature recited in exemplary Claim 17. For example, *Eickemeyer* does not teach or suggest a processor including:

> execution circuitry that performs at least said prefetch operation out-of-order with respect to said preceding instruction ..., wherein said execution circuitry performs said prefetch operation by calculating a speculative target memory address utilizing contents of at least one register without regard for whether said contents will be modified between calculation of said speculative target memory address and performing said register operation, ...

as recited in exemplary Claim 17 (and similarly in Claim 18).

With respect to the claimed execution circuitry, paragraph 12 of the present Office Action cites Figures 2-3 and col. 7, lines 22-25 and col. 8, lines 33-36 of *Eickemeyer*. However, blocks 304, 305 and 308 of Figure 3 of *Eickemeyer* and the accompanying description at col. 7, line 63 through column 8, line 3 clearly teaches that if a "pending load instruction...modifies a register used by the subject load instruction, the address generation from adder 205 will not be used" and no prefetch is performed (block 308). Thus, it is evident that *Eickemeyer* does not teach or suggest the calculation of a speculative target memory address "without regard for whether said contents [of the register] will be modified between calculation of said speculative target memory address and performing said register operation." Applicant therefore believes that that rejections of Claims 17 and 18 are overcome.

Having now responded to each objection and rejection set forth in the present Office Action, Applicant believes all pending claims are now in condition for allowance and respectfully requests such allowance.

No additional fee is believed to be required; however, in the event any additional fees are required, please charge IBM CORPORATION Deposit Account No. **09-0447**.

Respectfully submitted,

Brian F. Russell

Brian F. Russell
Registration No. 40,796
BRACEWELL & PATTERSON, LLP
P.O. Box 969
Austin, Texas 78767
(512) 472-7800
ATTORNEY FOR APPLICANT